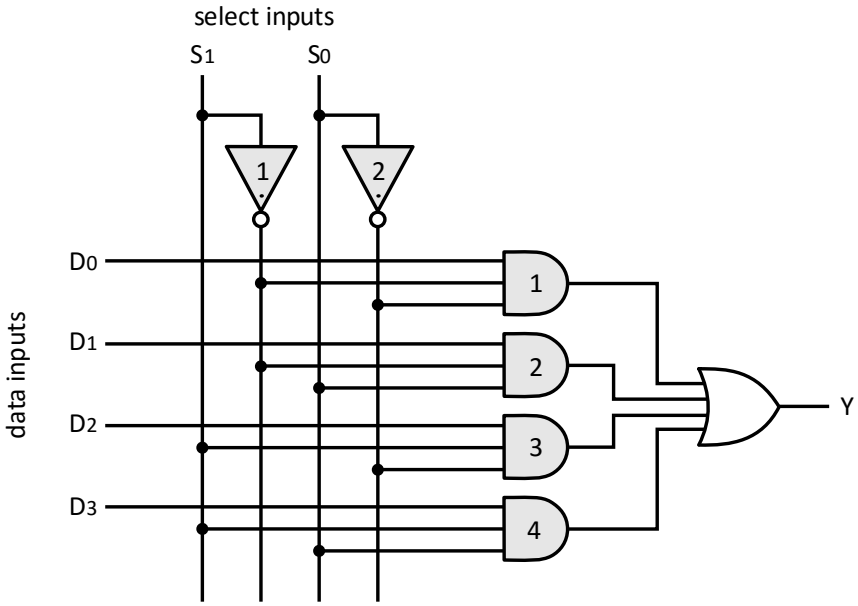
4.2.2 The 4:1 Line Multiplexer

This circuit has 4 data inputs. So its select inputs will be $2^2 = 4$ i.e. 2 select inputs. Its data inputs are denoted as D_3, D_2, D_1 and D_0, where D_3 is at MSB and D_0 is at LSB.

Its two select inputs are denoted by S_1 and S_0, where S_1 is at MSB and S_0 is at LSB. The circuit diagram is given below.



The Boolean equation of the circuit can be derived by finding out the output equations of each AND gate and then adding them together to get the final output Y.

1. The output equation of AND gate-1 is given by: $D_0.\overline{S_1}.\overline{S_0}$
2. The output equation of AND gate-2 is given by: $D_1.\overline{S_1}.S_0$
3. The output equation of AND gate-3 is given by: $D_2.S_1.\overline{S_0}$
4. The output equation of AND gate-4 is given by: $D_3.S_1.S_0$

So the final Boolean equation of OR gate at Y will be –

$$Y = D_0.\overline{S_1}.\overline{S_0} + D_1.\overline{S_1}.S_0 + D_2.S_1.\overline{S_0} + D_3.S_1.S_0$$

Thus as we apply the control signal at select inputs we can select to get a particular data input signal at the output as shown in following truth table.

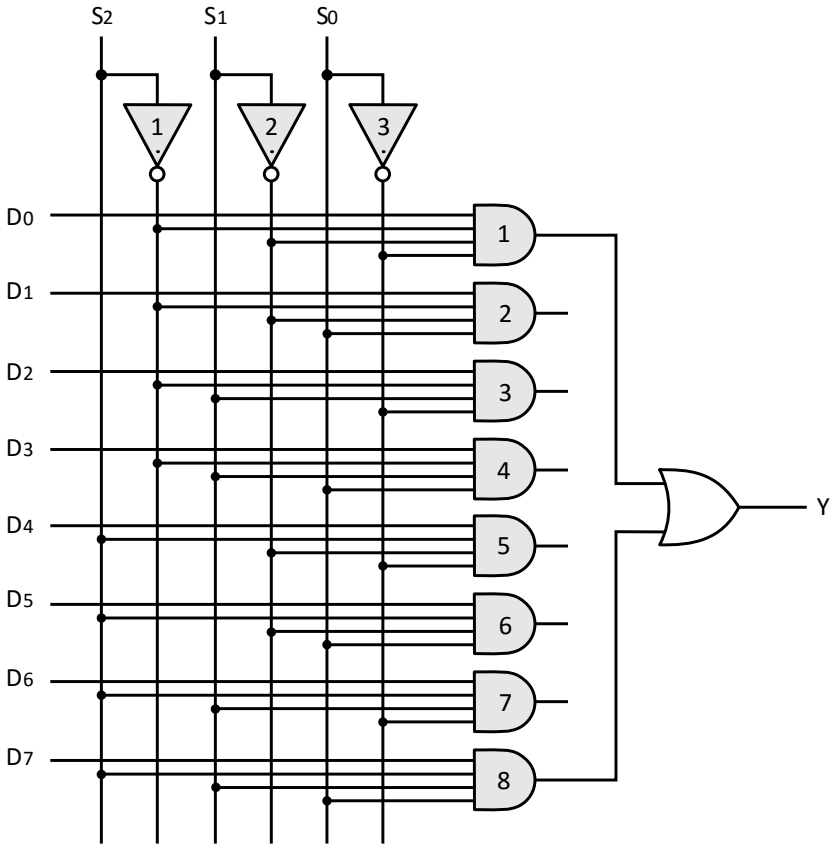
Select inputs		Signal available at output Y
S_1	S_0	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Truth table

4.2.3 The 8:1 Line Multiplexer

This circuit has 8 data inputs. So its select inputs will be $2^3 = 8$ i.e. 3 select inputs. Its data inputs are denoted as D_7, D_6, D_5, D_4, D_3, D_2, D_1 and D_0, where D_7 is at MSB and D_0 is at LSB.

Its three select inputs are denoted by S_2, S_1 and S_0, where S_2 is at MSB and S_0 is at LSB. The circuit diagram is given below.



The Boolean equation of the circuit is the addition of the outputs of AND gates at Y, as given below:

$$Y = D_0.\overline{S_2}.\overline{S_1}.\overline{S_0} + D_1.\overline{S_2}.\overline{S_1}.S_0 + D_2.\overline{S_2}.S_1.\overline{S_0} + D_0.\overline{S_2}.S_1.S_0$$
$$+D_0.S_2.\overline{S_1}.\overline{S_0} + D_0.S_2.\overline{S_1}.S_0 + D_0.S_2.S_1.\overline{S_0} + D_0.S_2.S_1.S_0$$

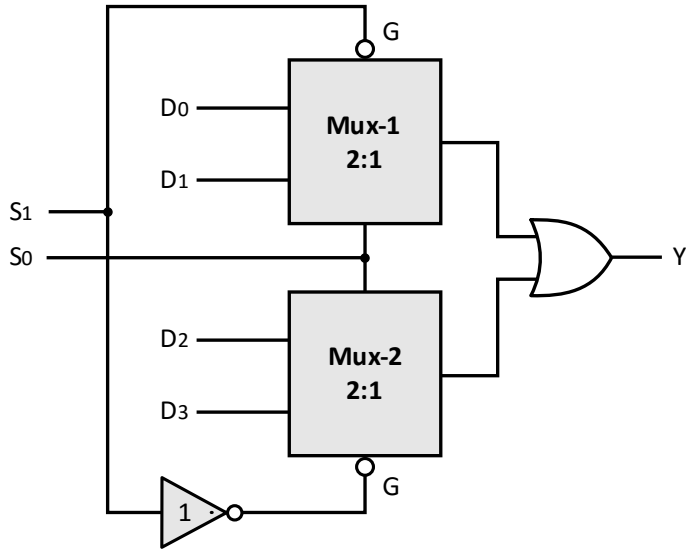
Using same method we can construct 16:1 line Mux and 32:1 line Mux, 64:1 line Mux and so on.

Important Note: To construct a Mux, the number of data inputs must be even in number. Then calculate the number of select inputs required for the given data inputs. For this we can use the formula $2^m = n$. *The output terminals of all AND gates may not be connected to the OR gate*, but the first output and the last output must be connected. Such type of connections is called as *data bus*.

Select inputs			Y
S_2	S_1	S_0	
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

4.2.4 The 4:1 Line Mux using two 2:1 line Mux

We can combine two 2:1 line Mux circuits to obtain one 4:1 line Mux. For this we want to use two NOR gates and the 'strobe inputs' of each Mux, as shown in following circuit.



Here two identical 2:1 line Mux are connected with strobe inputs (G) in inverted condition. The Mux-1 has two data inputs D_0 and D_1 with one select input S_0.

Similarly Mux-2 has two data inputs D_2 and D_3 with same select input S_0. The two select inputs of each Mux are joined together to produce one common select input S_0. And the outputs of both Mux are connected to OR gate to obtain the combine output Y.

Thus the circuit has four possible conditions, as explained below:

Case #1: When $S_1 = 0$ and then only Mux-1 works in normal way and Mux-2 remains inactive. So at its output we get either D_0 or D_1.

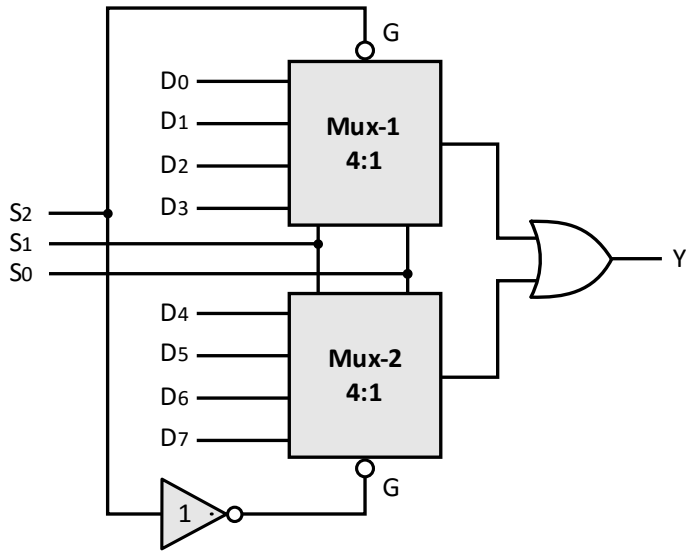
Case #2: When $S_1 = 1$, then only Mux-2 works in normal way and Mux-1 remains inactive. So at its output we get either D_2 or D_3.

Thus we can select only one Mux at a time and obtain the working of 4:1 line Mux by using two 2:1 line Mux circuits. The Boolean equation and truth table of the circuit is given below:

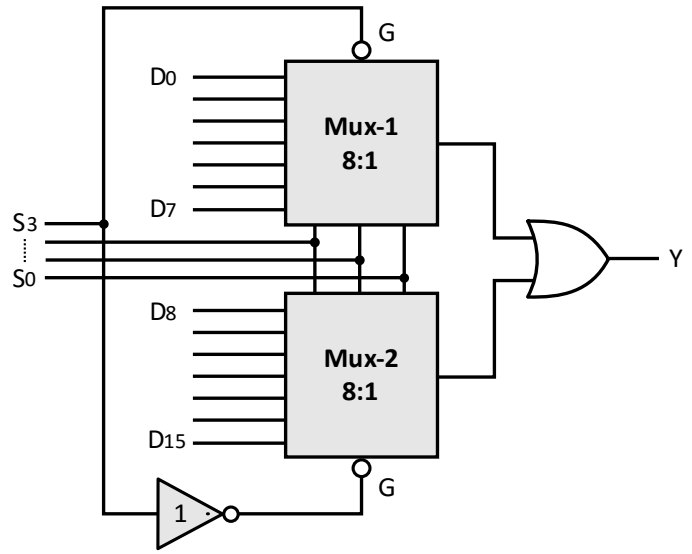
$$Y = D_0.\overline{S_1}.\overline{S_0} + D_1.\overline{S_1}.S_0 + D_2.S_1.\overline{S_0} + D_3.S_1.S_0$$

Select inputs		Signal available at output Y
S_1	S_0	
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

4.2.5 The 8:1 Line Mux using two 4:1 line Mux



4.2.6 The 16:1 Line Mux using two 8:1 line Mux



In this way we can create any type of Mux by using two identical Mux as explained in above topics.

Important Note: *In HSC board examination, questions are asked on up to 16:1 line Mux. So students must prepare up to this type of combination*. Try to draw the circuit many times and make its good practice.

4.2.7 Applications of Mux (Solutions to HSC Board Questions)

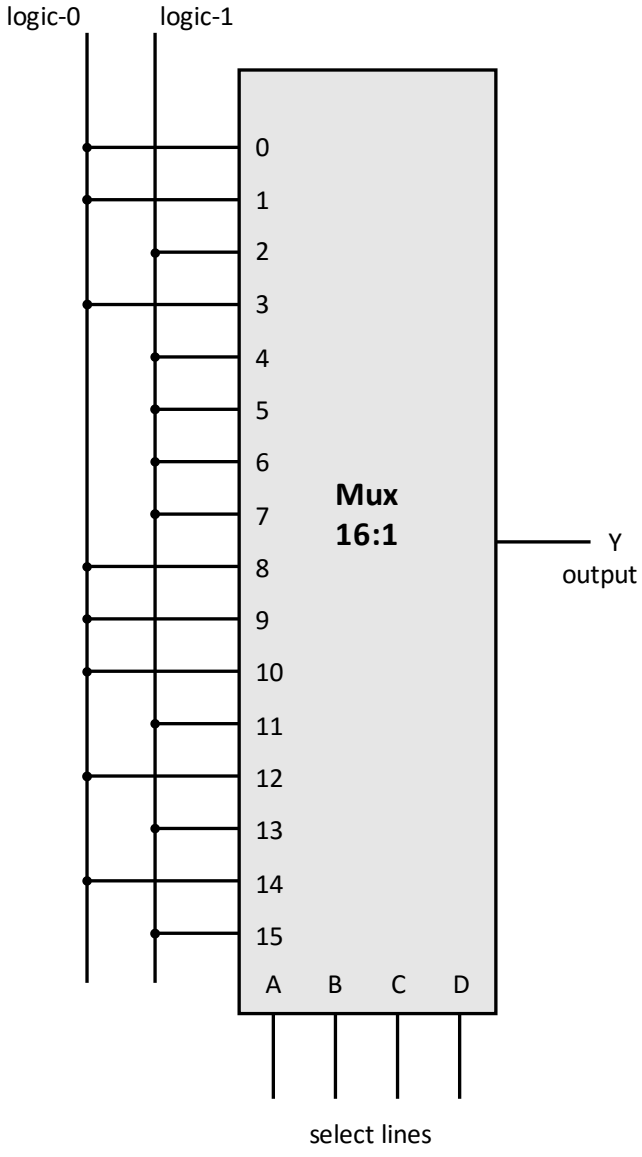
Example: Construct a combinational logic circuit using 16:1 line Mux by implementing the following expression:

$$f(A,B,C,D) = \Sigma_m(2,4,6,5,7,11,13,15)$$

Solution: There are four variables A, B, C, D in this expression. So we shall require 16:1 line Mux with 4 select inputs. We shall assume that the output of the Mux is active high.

Procedure:

1) Connect the active miniturms $(2,4,6,5,7,11,13,15)$ given in the bracket to logic-1.
2) Connect the inactive miniturms, which are not given in the bracket i.e. $(0,1,3,8,9,10,12,14)$ to logic-0.
3) Apply necessary control signal to select lines.
4) If the Mux outputs are active low, the interchange the logic-1 and logic-0 levels.



4.3 DEMULTIPLEXER

The demultiplexer is always used in combination with multiplexer to send and receive data in a long distance digital communication system.

Definition: Demultiplexer is defined as the type of CLC which has only one input but many outputs. In short it is called **one is to many** CLC. *It is also defined as data distributor CLC*.

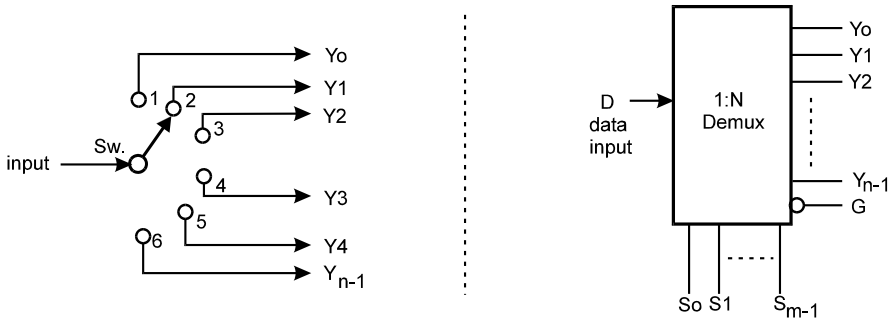
a) It has 'n' number of output terminals.
b) It has only one data input i.e. D.
c) It has 'm' number of control terminals i.e. select input terminals.
d) The number of output terminals and select input terminals are related as: $2^m = n$
e) Its outputs are denoted by $Y_0, Y_1, Y_2, Y_3 \ldots Y_{n-1}$ *where,* Y_0 *is at LSB position*.
f) Its select input terminals are denoted by $S_0, S_1, S_2, S_3 \ldots S_{m-1}$ *where,* S_0 *is at LSB position*.

Example: Suppose a demultiplexer circuit has 4 outputs. Then its number of select inputs will be 2. Its outputs will be denoted as Y_0, Y_1, Y_2, Y_3 and its select inputs will be denoted as S_0 & S_1. Such demultiplexer is called 1:4 line demultiplexer circuit.

4.3.1 Block Diagram of Demux

The following diagram *(left)* shows an equivalent arrangement of demultiplexer using a rotary switch. When the switch is rotated, the input signal is available at particular output.

In the same way, the general block diagram of demultiplexer *(right)* is shown. It has (D_{n-1}) number of outputs with only one input. Also it has (S_{m-1}) number of select inputs.



In right figure, when all select inputs are 00000…, then input signal D is available at Y_0 only. Similarly when all select inputs are 11111…, then the input signal D is available at Y_{n-1} output.

4.3.2 The 1:4 Line Demultiplexer

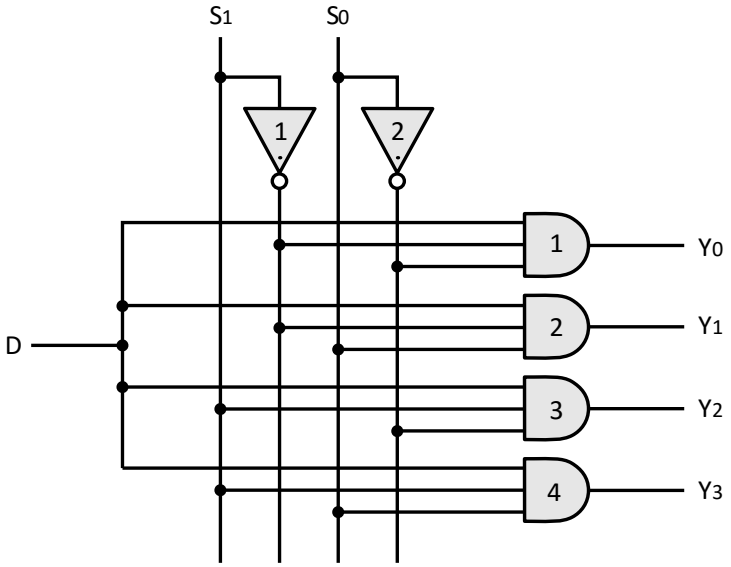
This circuit has 4 outputs. So its select inputs will be $2^2 = 4$ i.e. 2 select inputs. Its outputs are denoted as Y_0, Y_1, Y_2 and Y_3, where Y_3 is at MSB and Y_0 is at LSB. It has only one input as D.

Its two select inputs are denoted by S_1 and S_0, where S_1 is at MSB and S_0 is at LSB. The circuit diagram is given below. The Boolean equation of each AND gate is given below:

1) The output equation of AND gate-1 is given by: $D.\overline{S_1}.\overline{S_0}$
2) The output equation of AND gate-2 is given by: $D.\overline{S_1}.S_0$
3) The output equation of AND gate-3 is given by: $D.S_1.\overline{S_0}$
4) The output equation of AND gate-4 is given by: $D.S_1.S_0$

So the final Boolean equations at each output will be –

$$Y_0 = D.\overline{S_1}.\overline{S_0} \qquad Y_1 = D.\overline{S_1}.S_0 \qquad Y_2 = D.S_1.\overline{S_0} \qquad Y_3 = D.S_1.S_0$$



Thus as we apply the control signal at select inputs we can select to get the input signal at the particular output as shown in following truth table.

Select inputs		Input signal D available at
S_1	S_0	
0	0	Y_0
0	1	Y_1
1	0	Y_2
1	1	Y_3

Truth table

Important Note: *In the same way, we can construct any demultiplexer circuit like 1:2, 1:8, 1:16, etc. by modifying the basic circuit of Mux.*

EXERCISE 4.1 (ALL QUESTIONS ASKED IN BOARD EXAM)

1) Draw the circuit of 2:1, 16:1, 32:1 line Mux using gates and write its Boolean equations and truth table also.
2) Draw block diagram of 32:1 line Mux by using two 16:1 line Mux circuits? Explain its working with truth table and Boolean equation.
3) Implement the following Boolean expressions by using suitable Mux:

   (a) $f(A) = \Sigma_m(0)$ (b) $f(P,Q,R) = \Sigma_m(1,3,6,7,2)$ (c) $f(A,B) = \Sigma_m(0,2,3)$

4) Draw the circuit of 1:2, 1:8 and 1:16 line demux circuits using gates. Also write down its Boolean equations and the truth table.

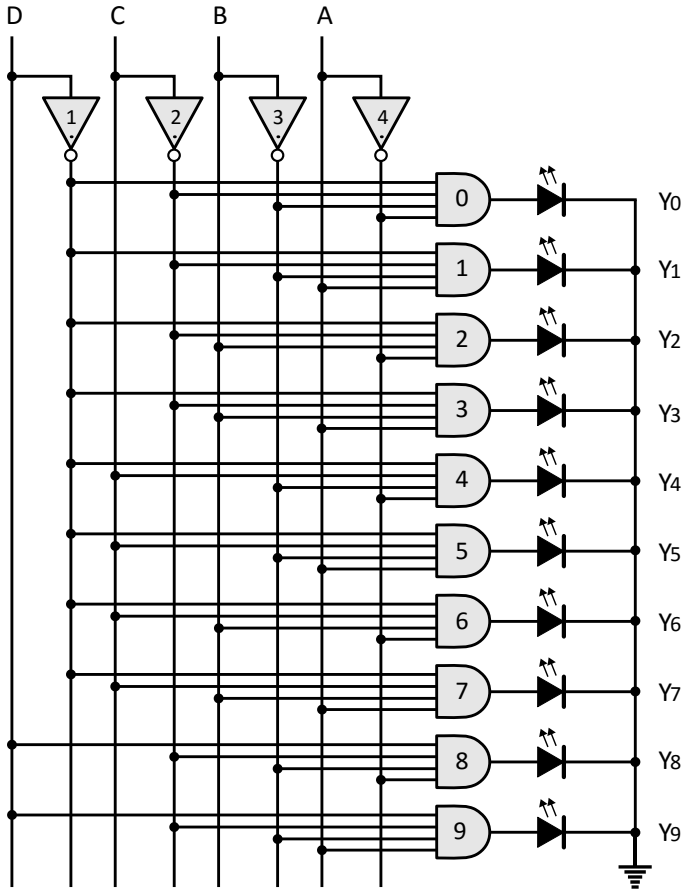
4.5 DECODER

Decoder is a combinational logic circuit, which converts binary signal into its equivalent decimal form. Hence, the circuit is also called as BCD to decimal decoder.

4.5.1 Decoder using basic gates

In this circuit, we use basic gates only to convert input of binary signal into its equivalent decimal value, as shown below.

Definition: *Decoder is a combinational logic circuit, which converts binary value into decimal form*. Hence, the circuit is also called as BCD to decimal decoder. A decoder is the opposite of encoder. If the output of encoder is DIRECTLY connected to input of decoder, then we get input = output.



Binary inputs				Outputs
D	***C***	***B***	***A***	
0	0	0	0	$Y_0 = 1$
0	0	0	1	$Y_1 = 1$
0	0	1	0	$Y_2 = 1$
0	0	1	1	$Y_3 = 1$
0	1	0	0	$Y_4 = 1$
0	1	0	1	$Y_5 = 1$
0	1	1	0	$Y_6 = 1$
0	1	1	1	$Y_7 = 1$
1	0	0	0	$Y_8 = 1$
1	0	0	1	$Y_9 = 1$

Truth table

In this circuit there are 10 AND gates with 4-inputs each. The inputs of each AND gate are connected in a particular combination, to the 8-line network. Out of 8-lines 4-lines are directly connected to input terminals $DCBA$ and other 4-lines are connected to the outputs of 4 NOT gates, which are $\bar{D}\bar{C}\bar{B}\bar{A}$. The outputs of the circuit are taken as $Y_0 - Y_9$. With the help of decoder we can visualize the output in sequential decimal format or in digital format.

Working: Suppose we apply, $DCBA = 0111$, then all the inputs of AND gate-7 will receive '1' and so the LED at its output will glow to show that the binary code 0111 is converted into decimal value 7. Similarly, if we apply $DCBA = 0011$, the all inputs of AND gate-3 will receive '1' and its output will become '1' to glow the LED. In this way, the circuit converts any binary from 0000 to 1001 into its equivalent decimal value of 0 to 9.

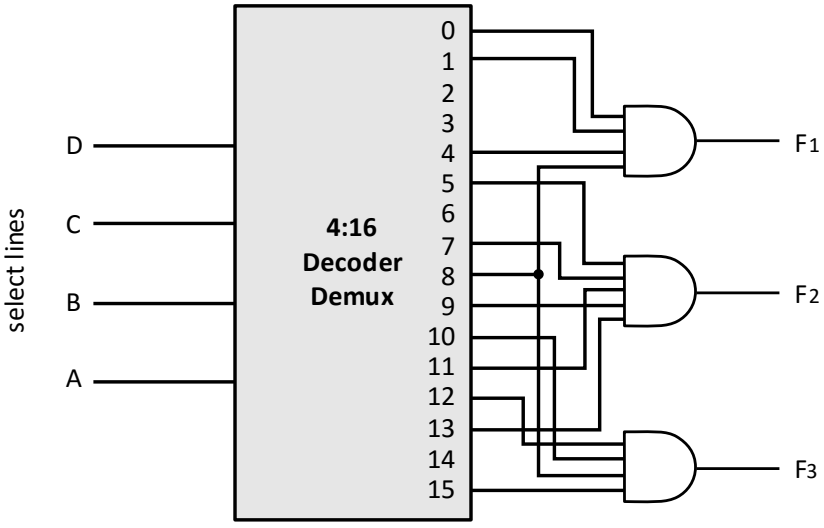
4.5.3 Applications of Decoder-Demultiplexer

The decoder-demultiplexer circuits can be used to implement complex Boolean equations for multipoint combinational logic. We shall see a typical example of such Boolean equations and its implementation.

Example: Implement the following multipoint combinational circuit using 4:16 line decoder-demultiplexer with active high outputs.

$$F_1 = \sum_m (0,1,4,8) \qquad F_2 = \sum_m (5,7,9,11,13) \qquad F_3 = \sum_m (8,10,12,15)$$

Solution: There are three outputs F_1, F_2 and F_3 in the given equations. All the outputs are active high, hence we shall use NAND gates for the combinational logic. Also the miniturms contain highest value as 15. So we shall use 4:16 line decoder-demultiplexer circuit, as shown below.



Important Note: In this same way, any multipoint combinational logic equation can be implemented as shown in above circuit. Remember following important points about this implementation.

1) If **active high** outputs are asked then use only NAND gates without bubbles, as shown in above circuit.
2) If **active low** outputs are asked in the question, then use bubbles i.e. NOT gates at each output of the circuit, as shown below.