MARCH 2008, DIGITAL ELECTRONICS, PAPER 2

Ques 1 (A): Select correct alternative and rewrite the following sub question – (4 Marks)

    a) The equivalent decimal number of a maximum highest binary number of length one byte is _____

(i) 128   **(ii) 127**   **(iii) 255**   **(iv) 256**

    b) An AND gate in positive logic becomes _____ gate in negative logic.

(i) OR   **(ii) NOR**   **(iii) NOT**   **(iv) NAND**

    c) Shift Register belongs to the class of _____

(i) Combinational logic circuit   **(ii) Sequential logic circuit**   **(iii) Both i) and ii)**   **(iv) None of the above**

    d) In a _____ type ADC, more than one comparators are used.

(i) Successive Approximation   **(ii) Simultaneous**   **(iii) Counter**   **(iv) None of the above**

Ques 1 (B): Attempt any TWO of the following – (6 Marks)

    a) Subtract the following numbers by using 2s complement method :
        i) $(11011)_2 – (011)_2$ ii) $(10111)_2 – (110001)_2$

    b) Convert the following :
        i) $(11011)_2 = (?)_{10}$ ii) $(F6.C9)_{16} = (?)_2$ iii) $(110\ 110\ 110.\ 110)_2 = (?)_{16}$

Ques 2 (A): Attempt any TWO of the following – (6 Marks)

    a) What are Universal Building Blocks ? How the basic gates are constructed using NOR gates only?

    b) Simplify the following: Y = ABC + ABC +ABC, Draw the logic diagram for simplified expression.

    c) Explain the working of clocked SR flip-flop using NAND gates.

Ques 2 (B): Attempt any ONE of the following – (4 Marks)

    a) Define radix or base of a number system. Explain with suitable example Hex-dabble method used for converting decimal number to hexadecimal number.

    b) What are the various codes used in digital system?
        What is their necessity? How many possible combinations are there in each code?

Ques 3 (A): Attempt any TWO of the following – (6 Marks)

    a) Explain the following parameters of digital ICs:
        i) Propagation delay   ii) Fan out   iii) Figure of merit.

    b) Explain the working of CMOS NOR gate with diagram.

    c) Explain the working 1:4 demultiplexer using logic gates.

Ques 3 (B): Attempt any ONE of the following – (4 Marks)

    a) State and prove De Morgan's Theorems.

    b) Define full adder. Draw a logic diagram of full adder. Write its Boolean equations and truth table

Ques 4 (A): Attempt any TWO of the following –   **(6 Marks)**

    a) What is a Multiplexer? Design a 4:1 multiplexer using 2:1 multiplexers.
    b) What is a Decoder? Explain BCD to Decimal decoder using appropriate logic gate.
    c) Explain the need of Multiplexing and Demultiplexing.

Ques 4 (B): Attempt any ONE of the following –   **(4 Marks)**

    a) Draw a well labeled diagram of digital computer. Explain the function of each block.
    b) Name various input and output devices used in computer.

Ques 5 (A): Attempt any TWO of the following –   **(6 Marks)**

    a) Explain J-K flip-flop with the help of logic diagram.
    b) Draw circuit diagram of weighted resistor type DAC. Explain its working.
    c) Explain working of T flip-flop with suitable diagram.

Ques 5 (B): Attempt any ONE of the following –   **(4 Marks)**

    a) Explain the working of TTL NAND with open collector output.
    b) What will be the output voltage of a 4 bit R-2R ladder, corresponding to the binary. Given: Logic 0 corresponds to 0 volts and logic 1 corresponds to 8 volts.

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OR

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Ques 5 (A): Attempt any TWO of the following –   **(6 Marks)**

    a) Explain the working of counter type ADC.
    b) Explain the working of right shift register using D flip-flops.
    c) Explain the working of Decimal of BCD encoder using OR gates.

Ques 5 (B): Attempt any ONE of the following –   **(4 Marks)**

    a) Draw a neat block diagram of asynchronous decade counter. Explain its working.
    b) Implement the following multi-output combinational logic circuit using a 4 : 16 line decoder circuit.
       $F_1 = m(1,2,4,7,8,11,12,13)$
       $F_2 = m(2,3,9,11)$
       $F_3 = m(10,12,13,14)$

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